Image 2816

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Appln. Of:	SAEKI
Serial No.:	09/910,117
Filed:	July 20, 2001
For:	CLOCK CONTROLLING METHOD AND CIRCUIT
Group:	2816
Examiner:	LINH M. NGUYEN

DOCKET: NEC G226

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER

Dear Sir:

In connection with the above-entitled matter, enclosed please find the following:

1. Three copies of Appellant's Brief on Appeal and Appendix A under Rule 192; and

2. Credit Card Payment Authorization Form PTO-2038 in the amount of $320.00 to cover the cost of filing the Appeal Brief.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account No. 08-1391.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: MAIL STOP APPEAL BRIEF - PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 12, 2004 at Tucson, Arizona.

By Nayat Mehalawi

NPS/ALK:nm

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APPELLANT'S BRIEF ON APPEAL

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APPELLANT'S BRIEF ON APPEAL

This Brief is being filed in support of Appellant's Appeal from the Final Rejection by the Examiner to the Board of Appeals and Interferences, the Notice of which was timely filed under Certificate of Mailing on November 10, 2003

REAL PARTY IN INTEREST

The Real Party in Interest in this Application is NEC Electronics Corporation, which has a place of business at 1753 Shimonumabe, Nakahara-ku, Kawasaki, Kanagawa, JAPAN 211-8668. NEC Electronics Corporation received an Assignment of all right, title and interest in the Application through an Assignment executed by NEC Corporation on November 1, 2002. The Assignment to NEC Electronics Corporation was submitted to the U.S. Patent and Trademark Office for recordation on February 11, 2003. The Assignment to NEC Electronics Corporation

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was recorded in the U.S. Patent and Trademark Office on February 19, 2003 at Reel 013736, Frame 0321. NEC Corporation, which has a place of business at 7-1, Shiba 5-chome, Minato-ku, Tokyo, JAPAN received an Assignment of all right, title and interest in the Application through an Assignment executed by the inventor, Takanori Saeki, on July 12, 2001 and by virtue of his employment by NEC Corporation. The Assignment to NEC Corporation was recorded in the U.S. Patent and Trademark Office on July 20, 2001 at Reel 012011, Frame 0216.

RELATED APPEALS AND INTERFERENCES

To the best of the knowledge of the undersigned attorney and Appellant, there are no other appeals or interferences that would directly affect, or be directly affected by, or have a bearing on, the Board's decision in the present Appeal.

STATUS OF THE AMENDMENTS

Appellant's Amendment E under Rule 116[1] was not entered in this case, as it was deemed not to place the Application in order for allowance.

STATUS OF THE CLAIMS ON APPEAL

Claims 1, 28, 29, 31 and 33-35 are pending in the current Application. Claims 33-35 have been allowed. Claims 1, 28, 29 and 31 stand finally rejected and are on Appeal. The claims on Appeal are set forth in **Appendix A** attached hereto.

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1. Amendment E under Rule 116 contained remarks only. No claim changes were proposed. Notwithstanding, the Examiner refused entry!

BACKGROUND OF THE INVENTION ON APPEAL

A PLL (phase locked loop) circuit is a feedback type circuit used to adjust clock period. A conventional PLL circuit includes a phase frequency detector (PFD) that receives an external clock signal and a signal supplied from a frequency divider. A charge pump receives an up signal and a down signal both output from a PFD and outputs a voltage corresponding to a phase difference. A loop filter receives the voltage from the charging pump to output smoothed voltage which is supplied as a control voltage to the voltage-controlled oscillator. And, an output clock signal of a frequency corresponding to the control voltage from the voltage-controlled oscillator is fed to a frequency divider. (Specification, page 1, lines 9-20).

However, in a conventional circuit, the phase adjustment operation is time-consuming and a jitter phase noise, which is inherent in a feedback system, is introduced. Moreover, a conventional programmable delay generator requires a power source voltage generating circuit, such as a threshold voltage generating circuit, which increases the circuit scale. (Specification, page 2, lines 13-21).

SUMMARY OF THE INVENTION ON APPEAL

The invention on Appeal is a clock controlling method and circuit that provides a clock control circuit and a clock control method that achieves highly accurate non-integer frequency conversions employing an eloquently simplified circuit configuration. In such a configuration, a clock is input into the clock control circuit, and the clock control circuit outputs a clock having a phase difference relative to the input clock. The phase difference between the clock input into the clock circuit and the output clock is obtained by adding or subtracting to or from the phase of the input clock by a predetermined unit value of a phase differential on each cycle. The unit

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value of phase differential is set by a control signal input into the clock control circuit. (Specification, page 3, lines 3-20).

ISSUES PRESENTED ON APPEAL

The issues presented on Appeal are:

(1) Whether claims 1, 28 and 31 are unpatentable under 35 USC § 102(e) as anticipated by Takemae et al. (U.S. Patent No. 6,194,932); and

(2) Whether claim 29 is unpatentable under 35 USC § 103(a) over Takemae et al. in view of Tanis et al. (U.S. Patent 5,258,724).

THE FINAL ACTION

In finally rejecting the claims on Appeal, the Examiner states the following:

> 2. Claims 1, 28, and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Takemae et al. (U.S. Patent No. 6,194,932).
>
> With respect to claims 1 and 28, Takemae et al. discloses, in Figures 2 and 3, a clock control circuit and a corresponding control method comprising means for generating and outputting an output clock having a phase relative to a reference clock [CLK0] by adding or subtracting to or from the phase by a predetermined unit value of a phase differential on each clock cycle of the reference clock, which is an input clock or a clock derived from the input clock.
>
> With respect to claim 31, Takemae et al. discloses, in Figures 2 and 3, that the unit phase difference is variably set by a control signal [N9].

(Final Action, mailed August 11, 2003, page 2, cipher 2.)

> 4. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takemae et al. (U.S. Patent No. 6,194,932) in view of Tanis et al. (U.S. Patent No. 5,258,724).

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> With respect to claim 29, Takemae et al. discloses all of the claimed limitations, as expressly recited in claim 28, except for specifying that the output clock of a frequency corresponding to a non-integer frequency with respect to the frequency of the reference clock can be outputted. Tanis et al. discloses, in figure 2, a fractional division synthesizer comprising a fractional (or non-integer) divider, which is capable of outputting the output clock of a frequency corresponding to a non-integer frequency with respect to the frequency of the reference clock. To implement a fractional divider fed with the input (reference) clock or the output clock of the circuit Takemae et al. to obtain high frequency resolution would have been obvious to one of ordinary skills in the art at the time of the invention since such a configuration would provide finer resolution than integer dividers, which has been a well-known practice in the art as evidenced by the teachings of Tanis et al..

(Final Action, mailed August 11, 2003, page 3, cipher 4.)

In his remarks, the Examiner states that:

> With respect to the Applicant's argument on claim s [sic] 1, 28 and 31, at page 1, the Examiner disagree with the Applicant's statement of *'Claims 1, 28, and 31 require that the phase be adjusted by a predetermined unit value of a phase differential on each clock cycle of the referenced clock. Takemae et al does not teach this feature..., in the instant claimed invention, as shown, e.g., in Fig. 2, each cycle of the clock is shifted by a predetermined amount causing an increase in the phase shift after each cycle as can be shown by the exemplary shift $\Delta\Phi$, $2\Delta\Phi$, and $3\Delta\Phi$.'* First, the Examiner disagrees with the part stating that *'Claims 1, 28, and 31 require that the phase be adjusted by a predetermined unit value of a phase differential on each clock cycle of the referenced clock. Takemae et al does not teach this feature'*; as clearly shown in Figs. 2 and 3 of Takemae, each clock cycle of the reference clock [CLK0] is adjusted by a predetermined unit value of a phase differential as each clock cycle is shifted and resulted in the output clock. Second, the Examiner disagrees with the Applicant's statement that the reference fails to show certain features of applicant's invention, '*each cycle of the clock is shifted by a predetermined amount causing an increase in the phase shift after each cycle as can be shown by the exemplary shift $\Delta\Phi$, $2\Delta\Phi$, and $3\Delta\Phi$.'*, it is noted that the features upon which applicant relies are not recited in the rejected claims. Although the claims are

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> interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Hence, claims 1, 28 and 31 remain anticipatorily rejected by Takemae."

(Final Action, mailed August 11, 2003, pages 4-5, cipher 7.)

GROUPING OF CLAIMS

Claims 1, 28, 29 and 31 are grouped together as containing the same essential patentable limitations, and thus stand or fall together.

THE REFERENCES

Takemae et al., U.S. Patent No. 6,194,932 ("Takemae et al.")

Takemae et al. teaches an improved delayed lock loop (DLL) circuit, which generates a timing signal to internal circuitry that operates with a fixed phase relative to an input clock.

In Takemae et al., an external clock CLK is supplied to an input buffer. The input buffer detects the external clock and generates an internal clock. A variable delay circuit delays the internal clock a predetermined time interval, and then generates a timing signal. A data output buffer is responsive to this timing signal, outputting data from memory DATA as data output DQ.

Tanis et al., US Patent 5,258,724 ("Tanis et al.")

Tanis et al. teaches a fractional division frequency synthesizer comprising a digital ramp generator producing a digital correction ramp controlled by a frequency control programmer; a divide by N divider coupled to an output of a voltage controlled oscillator with the divider being controlled by the program, where N is a selected one of an integer and a fraction one or greater; a

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digital phase detector coupled to a reference clock and the output of the divider to provide a digital phase error signal; a digital adder coupled to an output of the ramp generator and the phase detector to produce a ramp corrected digital phase error signal; and circuit arrangement coupled to an output of the adder and a control input of the controlled oscillator to convert the ramp corrected digital phase error signal to a ramp corrected analog phase error signal to control the controlled oscillator and thereby provide a controlled frequency signal at the output thereof.

ARGUMENTS ON APPEAL

I. THE REJECTION OF CLAIMS 1, 28 and 31 UNDER 35 U.S.C. § 102(E) AS ANTICIPATED BY TAKEMAE ET AL. IS IMPROPER BECAUSE TAKEMAE ET AL. DOES NOT TEACH ALL OF THE FEATURES OF APPELLANT'S CLAIMS.

A. Takemae et al. Teaches a Circuit that Generates an Output Clock with a Fixed Phase Relative to an Input Clock, not a Circuit that Generates an Output Clock whose Phase is Obtained by Adding or Subtracting to or from the Phase of the Output Clock, as Required in Appellant's Independent Claims 1, 28 and 31.

The rejection of claims 1, 28 and 31 under 35 USC §102(e) as anticipated by Takemae et al. (U.S. Patent No. 6,194,932) is in error. MPEP §2131 provides that:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Takemae et al. explicitly states that:

> [this] invention relates to an improved delayed lock loop (DLL), which generates a timing signal to internal circuitry that operates at a fixed phase timing relative to an external clock, and to an integrated circuit device, which comprises a DLL circuit, the scale of the circuitry of which can be reduced by omitting a variable delay circuit.

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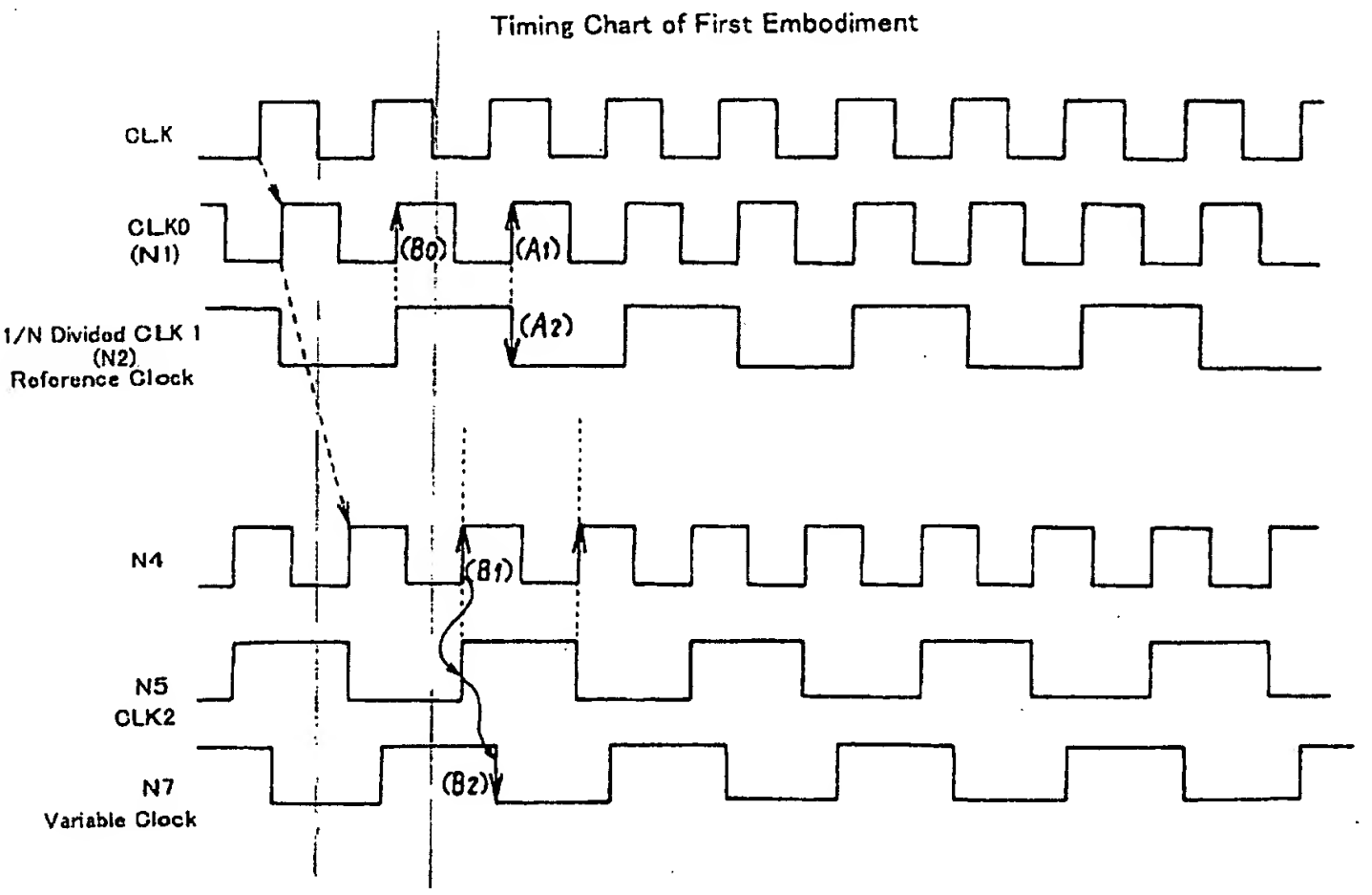
While the Examiner contends that Takemae et al. teaches: "Each clock cycle of the reference clock is adjusted by a predetermined unit value of a phase differential," (Final Action, mailed August 11, 2003, page 5, cipher 7), and Appellant agrees as this is inherent in a delay circuit, claim 1 inherently requires that the phase differential between the input and output clocks is variable.

This difference between Takemae et al. and Appellant's invention is best highlighted in FIG. 3 of Takemae et al. and Appellant's FIG. 2. In FIG. 3 of Takemae et al., reduced below and annotated for the convenience of the Board, the first rising edge of CLK and CLK0 corresponds to the second rising edge of N4 (the output clock of Takemae et al.), which represents a phase shift of the first clock cycle.



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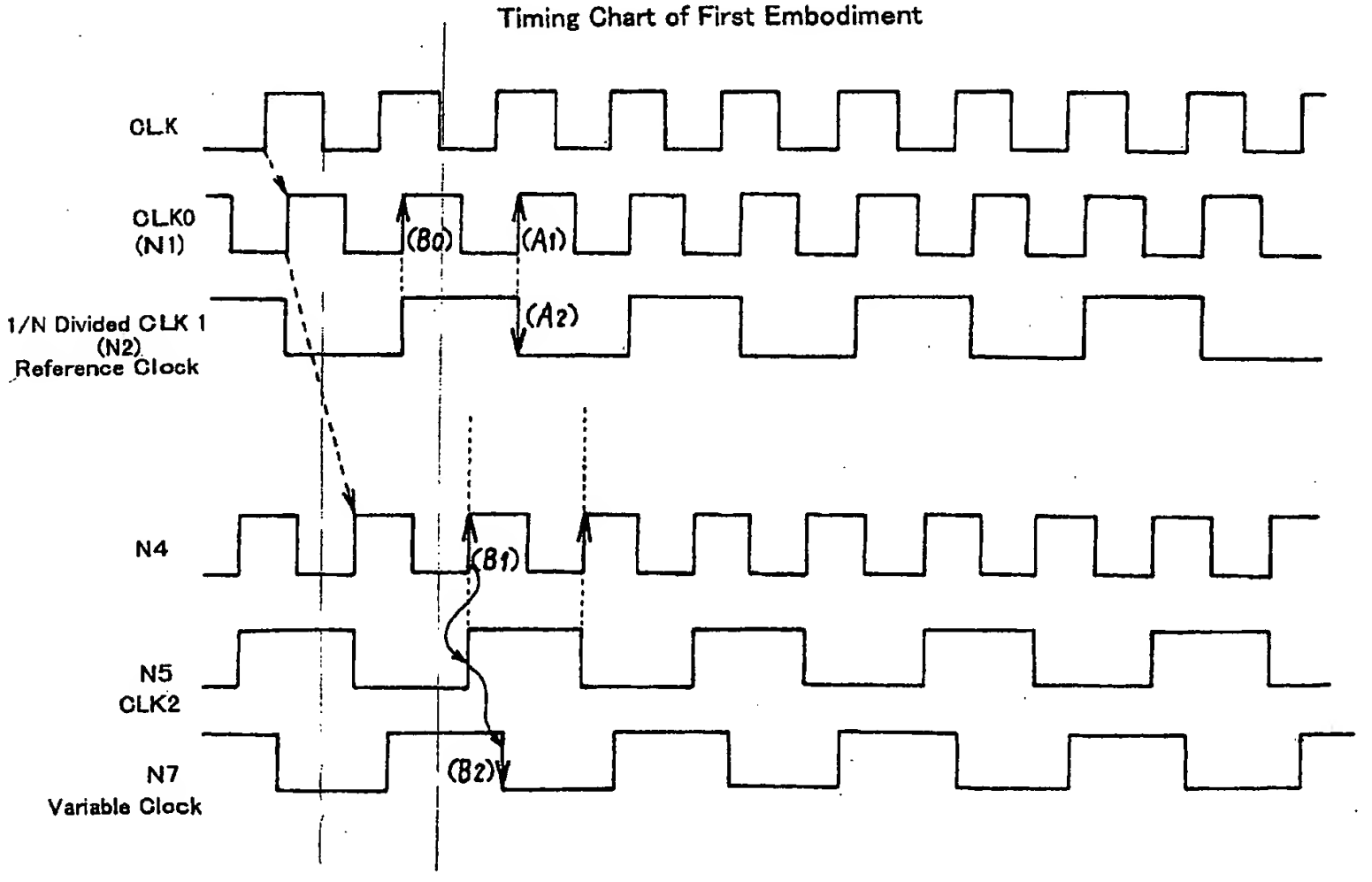
This difference between Takemae et al. and Appellant's invention is best highlighted in FIG. 3 of Takemae et al. and Appellant's FIG. 2. In FIG. 3 of Takemae et al., reduced below and annotated for the convenience of the Board, the first rising edge of CLK and CLK0 corresponds to the second rising edge of N4 (the output clock of Takemae et al.), which represents a phase shift of the first clock cycle.

FIG. 3

Timing Chart of First Embodiment



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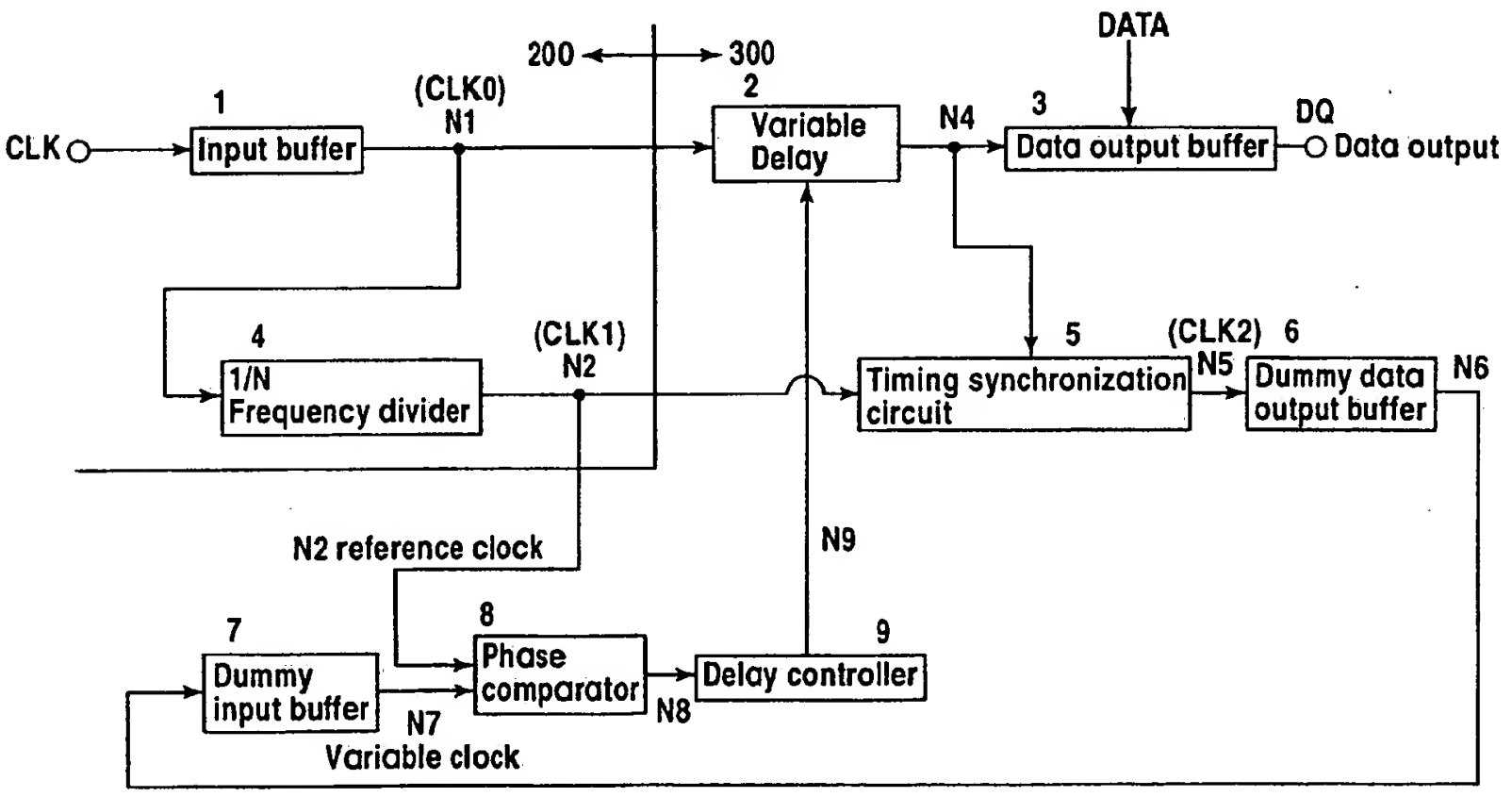
However, as shown in Appellant's FIG. 2, reduced below for the convenience of the Board, each clock cycle of the input clock shifts an output clock by a phase differential $\Delta\Phi$, resulting in the second output clock signal having a total phase shift of 2 $\Delta\Phi$, and the third output clock cycle having a total phase shift of 3 $\Delta\Phi$, and so forth.

FIG.2
First Embodiment



This difference is further highlighted in the accompanying Comparison Figure, reduced below for the convenience of the Board.

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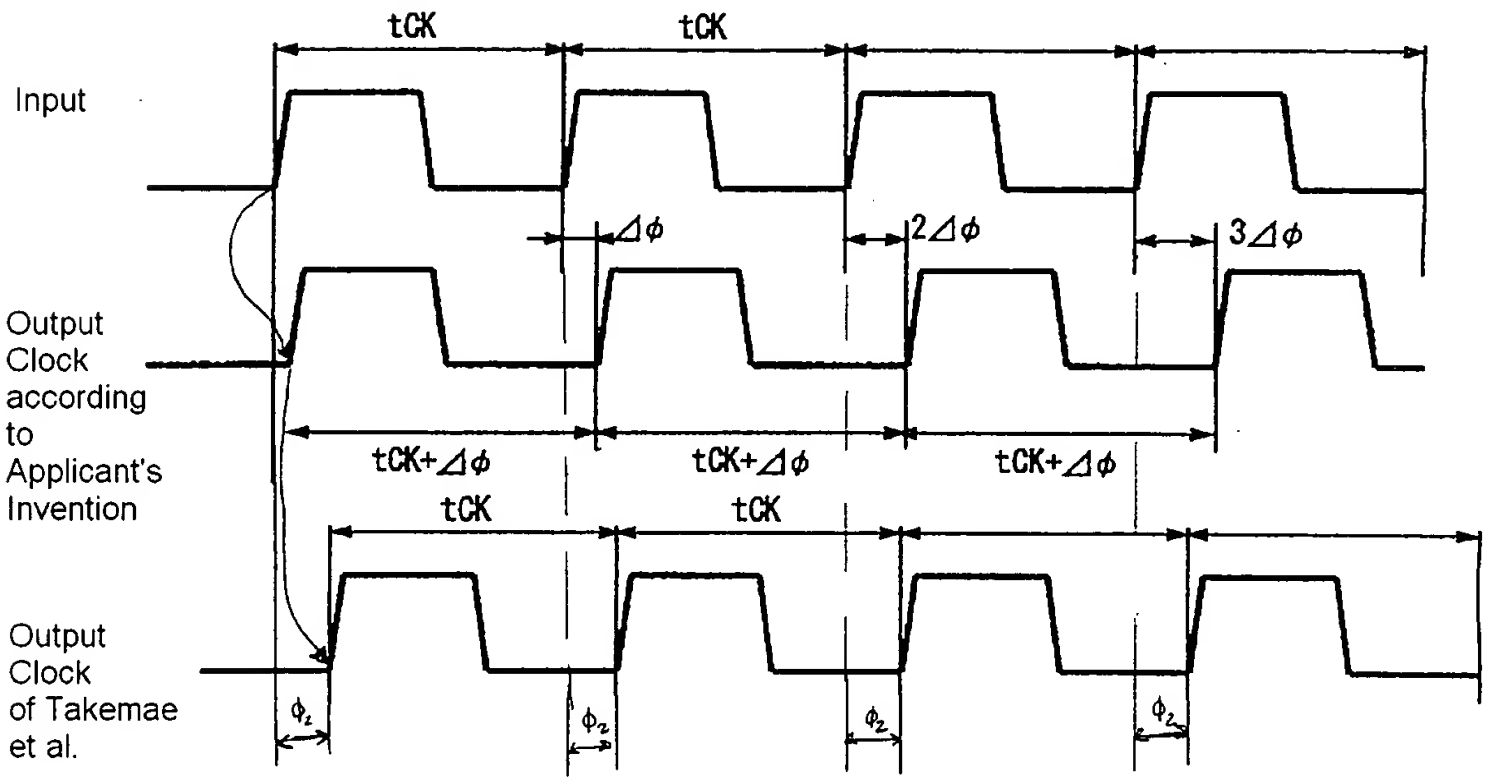
COMPARISON FIGURE



As the Board will note, the Comparison Figure shows that the output clock of Appellant's invention shifts each cycle of the clock input by $\Delta\Phi$, resulting in Appellant's output clock having a phase shift of 3 $\Delta\Phi$ at the rising edge of the fourth output clock cycle, and so forth. Alternatively, the input clock representative of Takemae et al. is shifted by $\Delta\Phi_2$ to generate the exemplary waveform, but no cycles of the output clock are additionally shifted, resulting in the output clock according to Takemae et al. having a phase shift of $\Delta\Phi_2$ at the rising edge of the fourth output clock cycle. Thus, the Board can clearly see how Takemae et al. cannot anticipate claims 1 or 28, or 31, which depends on claim 28.

B. The Examiner's Interpretation of Takemae et al. Ignores the Language of Appellant's Claim 1.

The Examiner in her Action states that "[I]n FIGS. 2 and 3 of Takemae et al., each clock cycle of the reference clock [CLK0] is adjusted by a predetermined unit value of a phase

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differential as each clock cycle is shifted and resulted in the output clock." (Final Action, p. 5, cipher 7). The Examiner then argues the Appellant's statement that "each cycle of the reference clock is shifted by a predetermined amount causing an increase in the phase shift after each cycle, as can be shown by the exemplary shift $\Delta\Phi$, $2\Delta\Phi$, and $3\Delta\Phi$... [are] features upon which Applicant relies [that] are not recited in the rejected claims." However, claim 1 specifically requires that the output clock have "a phase relative to a reference clock by adding or subtracting to or from said phase by a predetermined unit value of phase differential on each clock cycle of said reference clock." (emphasis added) Thus, in Appellant's claim 1, the phase of the output clock is added to or subtracted from on each clock cycle of the reference clock, not the input clock, as is required by the Examiner's interpretation. Clearly, the Examiner ignores the language of claim 1 to make her rejection, and the rejection of claims 1, 28, and 31 should not be maintained.

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II. THE REJECTION OF DEPENDENT CLAIM 29 UNDER 35 U.S.C. § 103(A) AS UNPATENTABLE OVER TAKEMAE ET AL. IN VIEW OF TANIS ET AL. IS IN ERROR BECAUSE THE COMBINATION OF TAKEMAE ET AL. AND TANIS ET AL. DOES NOT TEACH CLAIM 29.

As for the Examiner's rejection of claim 29 under 35 USC §103(a) as obvious over Takemae et al. in view of Tanis et al. (U.S. Patent No. 5,258,724), claim 29 is dependent on claim 28. Tanis et al. is only cited by the Examiner as teaching a fractional divider, and is acknowledged as so teaching. However, the deficiencies of the primary reference Takemae et al. vis-à-vis claim 28 are discussed above. Tanis et al. does not supply the missing teachings. Thus, no combination of Takemae et al. and Tanis et al. would achieve claim 28 or claim 29, which is dependent thereon. Thus, claim 29 is patentable for the reasons adduced above for claim 28, as well as for its own limitations.

CONCLUSION

In view of the foregoing, it is respectfully requested that the Examiner's Rejection of the subject Application be reversed in all respects.

Respectfully submitted,

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By Vajat Mushalame

NPS/ALK:nm

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APPENDIX A

CLAIMS ON APPEAL

Claim 1. A clock control circuit comprising:

a circuit for generating and outputting an output clock having a phase relative to a reference clock by adding or subtracting to or from said phase by a predetermined unit value of a phase differential on each clock cycle of said reference clock, said reference clock being an input clock or a clock derived from the input clock.

Claim 28. A clock control method comprising the steps of:

generating an output clock having a phase relative to a reference clock by adding or subtracting to or from said phase by a unit value of a phase differential on each clock cycle of said reference clock, said reference clock being an input clock or a clock derived from the input clock; and

outputting said output clock.

Claim 29. The clock control method as defined in claim 28 wherein the output clock of a frequency corresponding to a non-integer frequency with respect to the frequency of said reference clock can be output.

Claim 31. The clock control method as defined in claim 28 wherein the unit phase difference is variably set by a control signal.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Appln. Of:	SAEKI
Serial No.:	09/910,117
Filed:	July 20, 2001
For:	CLOCK CONTROLLING METHOD AND CIRCUIT
Group:	2816
Examiner:	LINH M. NGUYEN

DOCKET: NEC G226

MAIL STOP APPEAL BRIEF - PATENTS
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APPELLANT'S BRIEF ON APPEAL

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I. THE REJECTION OF CLAIMS 1, 28 AND 31 UNDER 35 U.S.C. § 102(E) AS ANTICIPATED BY TAKEMAE ET AL. IS IMPROPER BECAUSE TAKEMAE ET AL. DOES NOT TEACH OR RENDER OBVIOUS ALL OF THE FEATURES OF APPELLANT'S CLAIMS 7

A. Takemae et al. Teaches a Circuit that Generates an Output Clock with a Fixed Phase Relative to an Input Clock, not a Circuit that Generates an Output Clock whose Phase is Obtained by Adding or Subtracting to or from the Phase of the Output Clock, as Required in Appellant's Independent Claims 1, 28 and 31. 7

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II. THE REJECTION OF DEPENDENT CLAIM 29 UNDER 35 U.S.C. § 103(A) AS UNPATENTABLE OVER TAKEMAE ET AL. IN VIEW OF TANIS ET AL. IS IN ERROR BECAUSE THE COMBINATION OF TAKEMAE ET AL. AND TANIS ET AL. DOES NOT TEACH CLAIM 29. 11

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APPELLANT'S BRIEF ON APPEAL

This Brief is being filed in support of Appellant's Appeal from the Final Rejection by the Examiner to the Board of Appeals and Interferences, the Notice of which was timely filed under Certificate of Mailing on November 10, 2003

REAL PARTY IN INTEREST

The Real Party in Interest in this Application is NEC Electronics Corporation, which has a place of business at 1753 Shimonumabe, Nakahara-ku, Kawasaki, Kanagawa, JAPAN 211-8668. NEC Electronics Corporation received an Assignment of all right, title and interest in the Application through an Assignment executed by NEC Corporation on November 1, 2002. The Assignment to NEC Electronics Corporation was submitted to the U.S. Patent and Trademark Office for recordation on February 11, 2003. The Assignment to NEC Electronics Corporation

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was recorded in the U.S. Patent and Trademark Office on February 19, 2003 at Reel 013736, Frame 0321. NEC Corporation, which has a place of business at 7-1, Shiba 5-chome, Minato-ku, Tokyo, JAPAN received an Assignment of all right, title and interest in the Application through an Assignment executed by the inventor, Takanori Saeki, on July 12, 2001 and by virtue of his employment by NEC Corporation. The Assignment to NEC Corporation was recorded in the U.S. Patent and Trademark Office on July 20, 2001 at Reel 012011, Frame 0216.

RELATED APPEALS AND INTERFERENCES

To the best of the knowledge of the undersigned attorney and Appellant, there are no other appeals or interferences that would directly affect, or be directly affected by, or have a bearing on, the Board's decision in the present Appeal.

STATUS OF THE AMENDMENTS

Appellant's Amendment E under Rule 116[1] was not entered in this case, as it was deemed not to place the Application in order for allowance.

STATUS OF THE CLAIMS ON APPEAL

Claims 1, 28, 29, 31 and 33-35 are pending in the current Application. Claims 33-35 have been allowed. Claims 1, 28, 29 and 31 stand finally rejected and are on Appeal. The claims on Appeal are set forth in **Appendix A** attached hereto.

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1. Amendment E under Rule 116 contained remarks only. No claim changes were proposed. Notwithstanding, the Examiner refused entry!

BACKGROUND OF THE INVENTION ON APPEAL

A PLL (phase locked loop) circuit is a feedback type circuit used to adjust clock period. A conventional PLL circuit includes a phase frequency detector (PFD) that receives an external clock signal and a signal supplied from a frequency divider. A charge pump receives an up signal and a down signal both output from a PFD and outputs a voltage corresponding to a phase difference. A loop filter receives the voltage from the charging pump to output smoothed voltage which is supplied as a control voltage to the voltage-controlled oscillator. And, an output clock signal of a frequency corresponding to the control voltage from the voltage-controlled oscillator is fed to a frequency divider. (Specification, page 1, lines 9-20).

However, in a conventional circuit, the phase adjustment operation is time-consuming and a jitter phase noise, which is inherent in a feedback system, is introduced. Moreover, a conventional programmable delay generator requires a power source voltage generating circuit, such as a threshold voltage generating circuit, which increases the circuit scale. (Specification, page 2, lines 13-21).

SUMMARY OF THE INVENTION ON APPEAL

The invention on Appeal is a clock controlling method and circuit that provides a clock control circuit and a clock control method that achieves highly accurate non-integer frequency conversions employing an eloquently simplified circuit configuration. In such a configuration, a clock is input into the clock control circuit, and the clock control circuit outputs a clock having a phase difference relative to the input clock. The phase difference between the clock input into the clock circuit and the output clock is obtained by adding or subtracting to or from the phase of the input clock by a predetermined unit value of a phase differential on each cycle. The unit

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value of phase differential is set by a control signal input into the clock control circuit. (Specification, page 3, lines 3-20).

ISSUES PRESENTED ON APPEAL

The issues presented on Appeal are:

(1) Whether claims 1, 28 and 31 are unpatentable under 35 USC § 102(e) as anticipated by Takemae et al. (U.S. Patent No. 6,194,932); and

(2) Whether claim 29 is unpatentable under 35 USC § 103(a) over Takemae et al. in view of Tanis et al. (U.S. Patent 5,258,724).

THE FINAL ACTION

In finally rejecting the claims on Appeal, the Examiner states the following:

> 2. Claims 1, 28, and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Takemae et al. (U.S. Patent No. 6,194,932).
>
> With respect to claims 1 and 28, Takemae et al. discloses, in Figures 2 and 3, a clock control circuit and a corresponding control method comprising means for generating and outputting an output clock having a phase relative to a reference clock [CLK0] by adding or subtracting to or from the phase by a predetermined unit value of a phase differential on each clock cycle of the reference clock, which is an input clock or a clock derived from the input clock.
>
> With respect to claim 31, Takemae et al. discloses, in Figures 2 and 3, that the unit phase difference is variably set by a control signal [N9].

(Final Action, mailed August 11, 2003, page 2, cipher 2.)

> 4. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takemae et al. (U.S. Patent No. 6,194,932) in view of Tanis et al. (U.S. Patent No. 5,258,724).

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> With respect to claim 29, Takemae et al. discloses all of the claimed limitations, as expressly recited in claim 28, except for specifying that the output clock of a frequency corresponding to a non-integer frequency with respect to the frequency of the reference clock can be outputted. Tanis et al. discloses, in figure 2, a fractional division synthesizer comprising a fractional (or non-integer) divider, which is capable of outputting the output clock of a frequency corresponding to a non-integer frequency with respect to the frequency of the reference clock. To implement a fractional divider fed with the input (reference) clock or the output clock of the circuit Takemae et al. to obtain high frequency resolution would have been obvious to one of ordinary skills in the art at the time of the invention since such a configuration would provide finer resolution than integer dividers, which has been a well-known practice in the art as evidenced by the teachings of Tanis et al..

(Final Action, mailed August 11, 2003, page 3, cipher 4.)

In his remarks, the Examiner states that:

> With respect to the Applicant's argument on claim s [sic] 1, 28 and 31, at page 1, the Examiner disagree with the Applicant's statement of *'Claims 1, 28, and 31 require that the phase be adjusted by a predetermined unit value of a phase differential on each clock cycle of the referenced clock. Takemae et al does not teach this feature..., in the instant claimed invention, as shown, e.g., in Fig. 2, each cycle of the clock is shifted by a predetermined amount causing an increase in the phase shift after each cycle as can be shown by the exemplary shift $\Delta\Phi$, $2\Delta\Phi$, and $3\Delta\Phi$.'* First, the Examiner disagrees with the part stating that *'Claims 1, 28, and 31 require that the phase be adjusted by a predetermined unit value of a phase differential on each clock cycle of the referenced clock. Takemae et al does not teach this feature'*; as clearly shown in Figs. 2 and 3 of Takemae, each clock cycle of the reference clock [CLK0] is adjusted by a predetermined unit value of a phase differential as each clock cycle is shifted and resulted in the output clock. Second, the Examiner disagrees with the Applicant's statement that the reference fails to show certain features of applicant's invention, '*each cycle of the clock is shifted by a predetermined amount causing an increase in the phase shift after each cycle as can be shown by the exemplary shift $\Delta\Phi$, $2\Delta\Phi$, and $3\Delta\Phi$.*', it is noted that the features upon which applicant relies are not recited in the rejected claims. Although the claims are

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> interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Hence, claims 1, 28 and 31 remain anticipatorily rejected by Takemae."

(Final Action, mailed August 11, 2003, pages 4-5, cipher 7.)

GROUPING OF CLAIMS

Claims 1, 28, 29 and 31 are grouped together as containing the same essential patentable limitations, and thus stand or fall together.

THE REFERENCES

Takemae et al., U.S. Patent No. 6,194,932 ("Takemae et al.")

Takemae et al. teaches an improved delayed lock loop (DLL) circuit, which generates a timing signal to internal circuitry that operates with a fixed phase relative to an input clock.

In Takemae et al., an external clock CLK is supplied to an input buffer. The input buffer detects the external clock and generates an internal clock. A variable delay circuit delays the internal clock a predetermined time interval, and then generates a timing signal. A data output buffer is responsive to this timing signal, outputting data from memory DATA as data output DQ.

Tanis et al., US Patent 5,258,724 ("Tanis et al.")

Tanis et al. teaches a fractional division frequency synthesizer comprising a digital ramp generator producing a digital correction ramp controlled by a frequency control programmer; a divide by N divider coupled to an output of a voltage controlled oscillator with the divider being controlled by the program, where N is a selected one of an integer and a fraction one or greater; a

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digital phase detector coupled to a reference clock and the output of the divider to provide a digital phase error signal; a digital adder coupled to an output of the ramp generator and the phase detector to produce a ramp corrected digital phase error signal; and circuit arrangement coupled to an output of the adder and a control input of the controlled oscillator to convert the ramp corrected digital phase error signal to a ramp corrected analog phase error signal to control the controlled oscillator and thereby provide a controlled frequency signal at the output thereof.

ARGUMENTS ON APPEAL

I. THE REJECTION OF CLAIMS 1, 28 and 31 UNDER 35 U.S.C. § 102(E) AS ANTICIPATED BY TAKEMAE ET AL. IS IMPROPER BECAUSE TAKEMAE ET AL. DOES NOT TEACH ALL OF THE FEATURES OF APPELLANT'S CLAIMS.

A. Takemae et al. Teaches a Circuit that Generates an Output Clock with a Fixed Phase Relative to an Input Clock, not a Circuit that Generates an Output Clock whose Phase is Obtained by Adding or Subtracting to or from the Phase of the Output Clock, as Required in Appellant's Independent Claims 1, 28 and 31.

The rejection of claims 1, 28 and 31 under 35 USC §102(e) as anticipated by Takemae et al. (U.S. Patent No. 6,194,932) is in error. MPEP §2131 provides that:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Takemae et al. explicitly states that:

> [this] invention relates to an improved delayed lock loop (DLL), which generates a timing signal to internal circuitry that operates at a fixed phase timing relative to an external clock, and to an integrated circuit device, which comprises a DLL circuit, the scale of the circuitry of which can be reduced by omitting a variable delay circuit.

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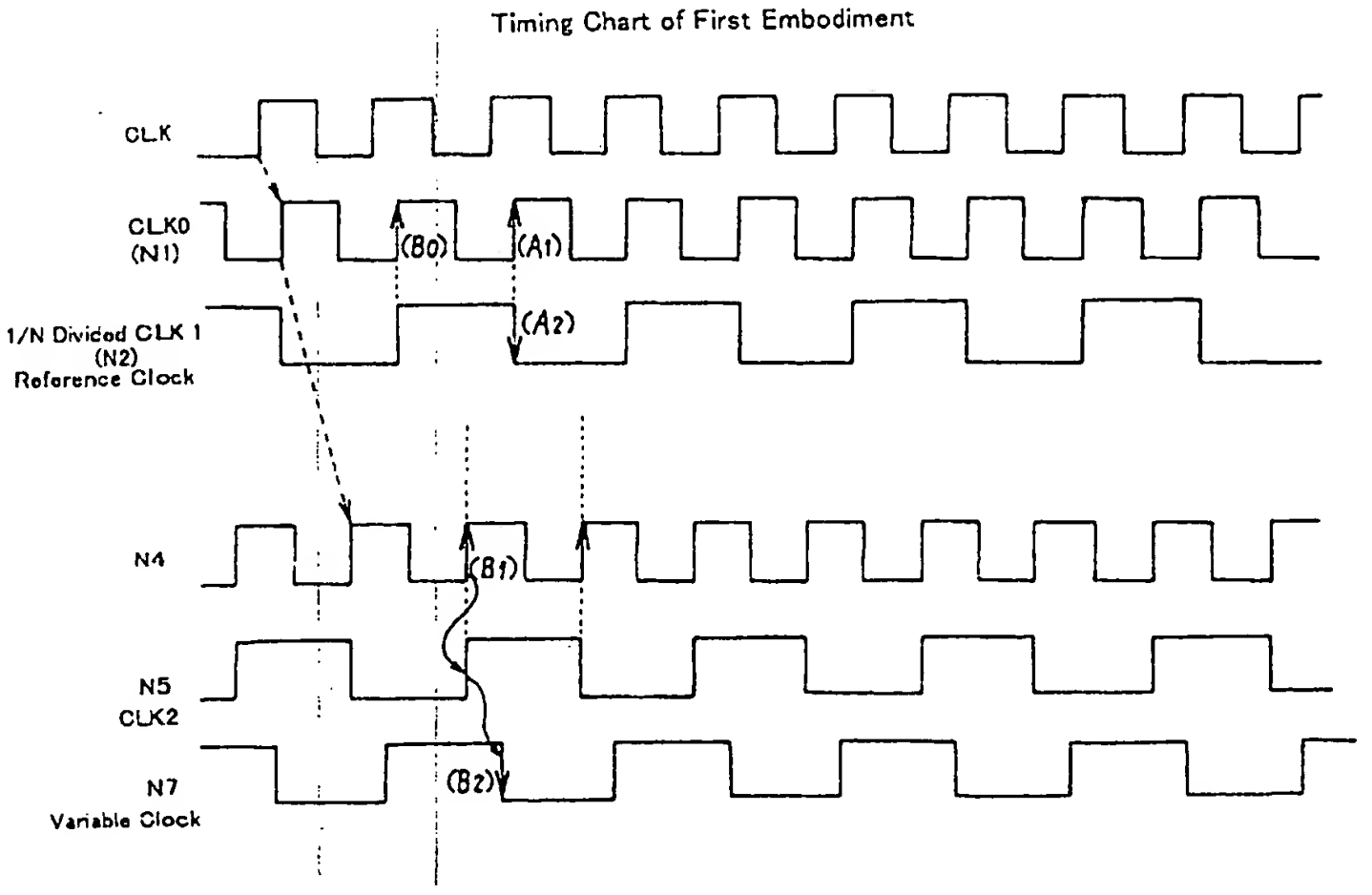
While the Examiner contends that Takemae et al. teaches: "Each clock cycle of the reference clock is adjusted by a predetermined unit value of a phase differential," (Final Action, mailed August 11, 2003, page 5, cipher 7), and Appellant agrees as this is inherent in a delay circuit, claim 1 inherently requires that the phase differential between the input and output clocks is variable.

This difference between Takemae et al. and Appellant's invention is best highlighted in FIG. 3 of Takemae et al. and Appellant's FIG. 2. In FIG. 3 of Takemae et al., reduced below and annotated for the convenience of the Board, the first rising edge of CLK and CLK0 corresponds to the second rising edge of N4 (the output clock of Takemae et al.), which represents a phase shift of the first clock cycle.



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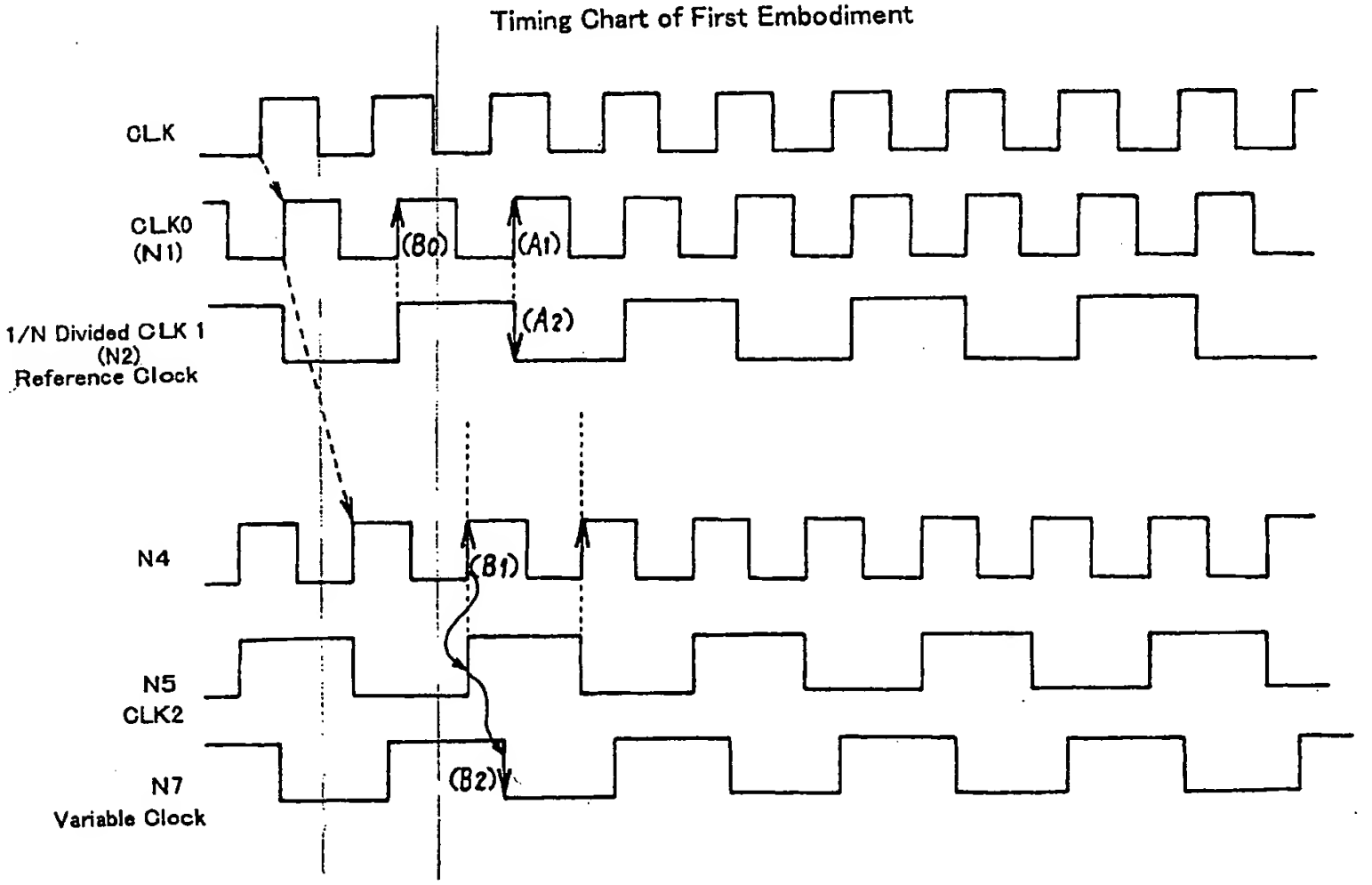
While the Examiner contends that Takemae et al. teaches: "Each clock cycle of the reference clock is adjusted by a predetermined unit value of a phase differential," (Final Action, mailed August 11, 2003, page 5, cipher 7), and Appellant agrees as this is inherent in a delay circuit, claim 1 inherently requires that the phase differential between the input and output clocks is variable.

This difference between Takemae et al. and Appellant's invention is best highlighted in FIG. 3 of Takemae et al. and Appellant's FIG. 2. In FIG. 3 of Takemae et al., reduced below and annotated for the convenience of the Board, the first rising edge of CLK and CLK0 corresponds to the second rising edge of N4 (the output clock of Takemae et al.), which represents a phase shift of the first clock cycle.

FIG. 3

Timing Chart of First Embodiment



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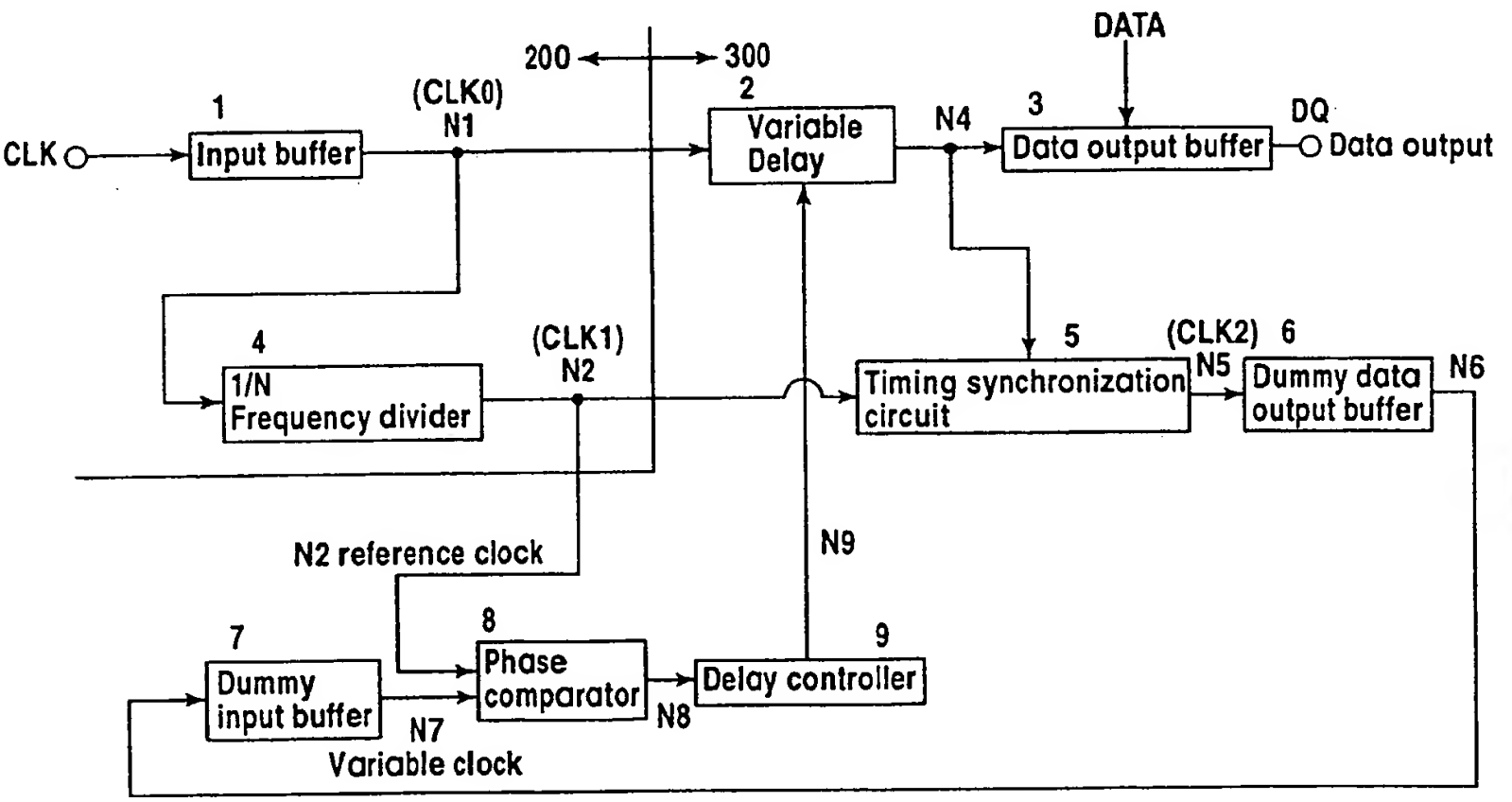
However, as shown in Appellant's FIG. 2, reduced below for the convenience of the Board, each clock cycle of the input clock shifts an output clock by a phase differential $\Delta\Phi$, resulting in the second output clock signal having a total phase shift of 2 $\Delta\Phi$, and the third output clock cycle having a total phase shift of 3 $\Delta\Phi$, and so forth.

FIG.2
First Embodiment



This difference is further highlighted in the accompanying Comparison Figure, reduced below for the convenience of the Board.

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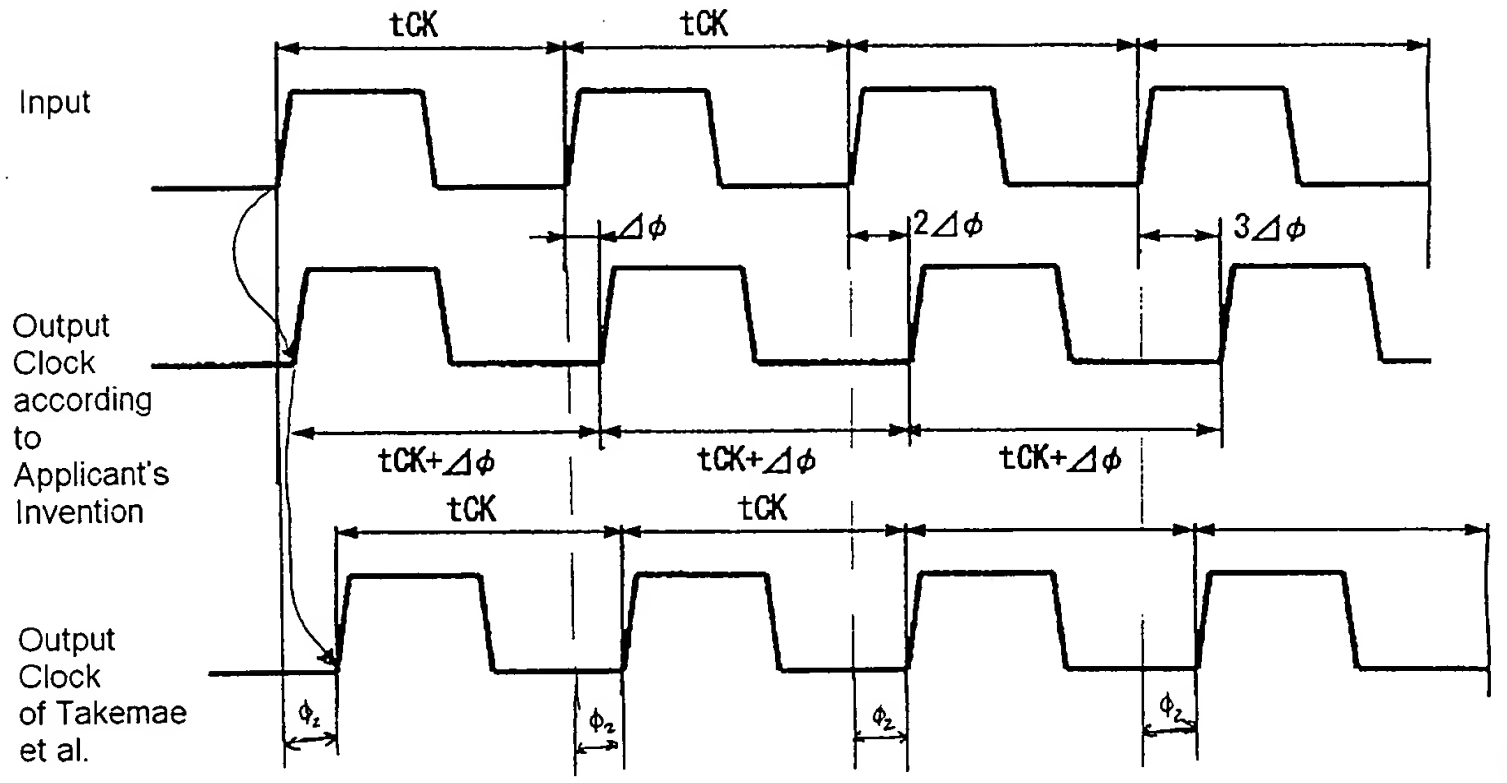
COMPARISON FIGURE



As the Board will note, the Comparison Figure shows that the output clock of Appellant's invention shifts each cycle of the clock input by $\Delta\Phi$, resulting in Appellant's output clock having a phase shift of 3 $\Delta\Phi$ at the rising edge of the fourth output clock cycle, and so forth. Alternatively, the input clock representative of Takemae et al. is shifted by $\Delta\Phi_2$ to generate the exemplary waveform, but no cycles of the output clock are additionally shifted, resulting in the output clock according to Takemae et al. having a phase shift of $\Delta\Phi_2$ at the rising edge of the fourth output clock cycle. Thus, the Board can clearly see how Takemae et al. cannot anticipate claims 1 or 28, or 31, which depends on claim 28.

B. The Examiner's Interpretation of Takemae et al. Ignores the Language of Appellant's Claim 1.

The Examiner in her Action states that "[I]n FIGS. 2 and 3 of Takemae et al., each clock cycle of the reference clock [CLK0] is adjusted by a predetermined unit value of a phase

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differential as each clock cycle is shifted and resulted in the output clock." (Final Action, p. 5, cipher 7). The Examiner then argues the Appellant's statement that "each cycle of the reference clock is shifted by a predetermined amount causing an increase in the phase shift after each cycle, as can be shown by the exemplary shift $\Delta\Phi$, $2\Delta\Phi$, and $3\Delta\Phi$... [are] features upon which Applicant relies [that] are not recited in the rejected claims." However, claim 1 specifically requires that the output clock have "a phase relative to a reference clock by adding or subtracting to or from said phase by a predetermined unit value of phase differential on each clock cycle of said reference clock." (emphasis added) Thus, in Appellant's claim 1, the phase of the output clock is added to or subtracted from on each clock cycle of the reference clock, not the input clock, as is required by the Examiner's interpretation. Clearly, the Examiner ignores the language of claim 1 to make her rejection, and the rejection of claims 1, 28, and 31 should not be maintained.

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II. THE REJECTION OF DEPENDENT CLAIM 29 UNDER 35 U.S.C. § 103(A) AS UNPATENTABLE OVER TAKEMAE ET AL. IN VIEW OF TANIS ET AL. IS IN ERROR BECAUSE THE COMBINATION OF TAKEMAE ET AL. AND TANIS ET AL. DOES NOT TEACH CLAIM 29.

As for the Examiner's rejection of claim 29 under 35 USC §103(a) as obvious over Takemae et al. in view of Tanis et al. (U.S. Patent No. 5,258,724), claim 29 is dependent on claim 28. Tanis et al. is only cited by the Examiner as teaching a fractional divider, and is acknowledged as so teaching. However, the deficiencies of the primary reference Takemae et al. vis-à-vis claim 28 are discussed above. Tanis et al. does not supply the missing teachings. Thus, no combination of Takemae et al. and Tanis et al. would achieve claim 28 or claim 29, which is dependent thereon. Thus, claim 29 is patentable for the reasons adduced above for claim 28, as well as for its own limitations.

CONCLUSION

In view of the foregoing, it is respectfully requested that the Examiner's Rejection of the subject Application be reversed in all respects.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: MAIL STOP APPEAL BRIEF - PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 12, 2004, at Tucson, Arizona.

By Nayat Mshalaine

NPS/ALK:nm

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APPENDIX A

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APPENDIX A

CLAIMS ON APPEAL

Claim 1. A clock control circuit comprising:

a circuit for generating and outputting an output clock having a phase relative to a reference clock by adding or subtracting to or from said phase by a predetermined unit value of a phase differential on each clock cycle of said reference clock, said reference clock being an input clock or a clock derived from the input clock.

Claim 28. A clock control method comprising the steps of:

generating an output clock having a phase relative to a reference clock by adding or subtracting to or from said phase by a unit value of a phase differential on each clock cycle of said reference clock, said reference clock being an input clock or a clock derived from the input clock; and

outputting said output clock.

Claim 29. The clock control method as defined in claim 28 wherein the output clock of a frequency corresponding to a non-integer frequency with respect to the frequency of said reference clock can be output.

Claim 31. The clock control method as defined in claim 28 wherein the unit phase difference is variably set by a control signal.

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